CLAIMS

1. A decoding apparatus for decoding LDPC (Low Density Parity Check) codes, when using as a sub-matrix, a (P × P) unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, said quasi-unit matrix, and said shift matrix, or a (P × P) 0-matrix, a check matrix of said LDPC codes is represented by a combination of a plurality of said sub-matrices, said decoding apparatus comprising:

first computation means for simultaneously performing P check node computations for decoding said LDPC codes; and

second computation means for simultaneously performing P variable node computations for decoding said LDPC codes.

2. The decoding apparatus according to Claim 1, wherein said first computation means has P check node calculators for performing check node computations, and

said second computation means has P variable node calculators for performing variable node computations.

3. The decoding apparatus according to Claim 1, further comprising:

message storage means for simultaneously reading and writing message data corresponding to P edges, which is

obtained as a result of said P check node computations or said P variable node computations.

4. The decoding apparatus according to Claim 3, wherein said message storage means stores message data corresponding to the edges, which are read during the check node computation in such a manner that 1s of the check matrix are packed closer in the row direction.

5. The decoding apparatus according to Claim 3, wherein said message storage means stores message data corresponding to edges, which are read during the variable node computation in such a manner that 1s of the check matrix are packed closer in the column direction.

6. The decoding apparatus according to Claim 3, wherein said message storage means stores, at the same address, messages corresponding to P edges belonging to a unit matrix whose weight is 1, a quasi-unit matrix, or a shift matrix when the sub-matrices whose weight is 2 or more from among the sub-matrices representing said check matrix are represented in the form of the sum of the unit matrix whose weight is 1, the quasi-unit matrix, or the shift matrix.

7. The decoding apparatus according to Claim 3, wherein said message storage means comprises number-of-rows/p FIFOs and number-of-columns/p FIFOs, and

said number-of-rows/p FIFOs and said number-of-columns/p FIFOs each have a number of words corresponding to

the weight of the row and the weight of the column of said check matrix, respectively.

8. The decoding apparatus according to Claim 3, wherein said message storage means comprises a RAM (Random Access Memory), and

said RAM stores said message data in the read-out sequence in such a manner as to be packed closer and reads said message data in the storage position sequence.

9. The decoding apparatus according to Claim 1, further comprising:

received information storage means for storing received information of LDPC codes and for simultaneously reading P pieces of said received information.

10. The decoding apparatus according to Claim 9, wherein said received information storage means stores said received information in such a manner that the received information can be read in the sequence necessary for said variable node computation.

11. The decoding apparatus according to Claim 1 further comprising:

rearranging means for rearranging messages obtained as a result of said P check node computations or said P variable node computations.

12. The decoding apparatus according to Claim 11, wherein said rearranging means comprises a barrel shifter.

13. The decoding apparatus according to Claim 1, wherein said first computation means and said second computation means determine messages corresponding to P edges.

14. The decoding apparatus according to Claim 1, wherein said first computation means performs some of said P check node computations and said P variable node computations, and

said second computation means performs some of the others of said P variable node computations.

15. The decoding apparatus according to Claim 14, wherein said first computation means comprises P calculators for performing some of said P check node computations and said P variable node computations, and

said second computation means comprises P calculators for performing some of the others of said P variable node computations.

16. The decoding apparatus according to Claim 14, further comprising:

first decoding in-progress result storage means for simultaneously reading and writing first decoding in-progress results corresponding to P edges, which are obtained by said first computation means by performing some of said P check node computations and said P variable node computations.

17. The decoding apparatus according to Claim 16, wherein said first decoding in-progress result storage means stores

said first decoding in-progress results corresponding to the edge, which are read when some of the others of said P variable node computations are performed, in such a manner that 1s of the check matrix are packed closer in the row direction.

18. The decoding apparatus according to Claim 16, wherein said first decoding in-progress result storage means are two single-port RAMs (Random Access Memories).

19. The decoding apparatus according to Claim 18, wherein said two single-port RAMs alternately store said first decoding in-progress results in units of said first decoding in-progress results corresponding to edges of P rows of said check matrix.

20. The decoding apparatus according to Claim 18, wherein said two single-port RAMs (Random Access Memories) each read said first decoding in-progress results stored at the same address.

21. The decoding apparatus according to Claim 16, wherein said first decoding in-progress result storage means stores, at the same address, said first decoding in-progress results corresponding to P edges belonging to a unit matrix whose weight is 1, a quasi-unit matrix, or a shift matrix when the sub-matrices whose weight is 2 or more from among the sub-matrices representing said check matrix are represented in the form of the sum of the unit matrix whose weight is 1,

the quasi-unit matrix, or the shift matrix.

22. The decoding apparatus according to Claim 14, further comprising:

second decoding in-progress result storage means for simultaneously reading and writing said second decoding in-progress results corresponding to P edges, which are obtained by said second computation means by performing some of the others of said P variable node computations.

23. The decoding apparatus according to Claim 14, further comprising:

received information storage means for storing received information of LDPC codes and simultaneously reading said P pieces of received information.

24. The decoding apparatus according to Claim 23, wherein said received information storage means stores said received information in such a manner that said received information can be read in the sequence necessary for some of the others of said P variable node computations.

25. The decoding apparatus according to Claim 14, further comprising:

rearranging means for rearranging first decoding in-progress results obtained by said first computation means by performing some of said P check node computations and said P variable node computations, or second decoding in-progress results obtained by said second computation means by

performing some of the others of said P variable node computations.

26. The decoding apparatus according to Claim 25, wherein said rearranging means comprises a barrel shifter.

27. The decoding apparatus according to Claim 1, wherein said first computation means performs some of said P check node computations, and

said second computation means performs some of the others of said P check node computations, and said P variable node computations.

28. The decoding apparatus according to Claim 27, wherein said first computation means comprises P calculators for performing some of said P check node computations, and

said second computation means comprises P calculators for performing some of the others of said P check node computations, and said P variable node computations.

29. The decoding apparatus according to Claim 27, further comprising:

first decoding in-progress result storage means for simultaneously reading and writing first decoding in-progress results corresponding to P edges, which are obtained by said first computation means by performing some of said P check node computations.

30. The decoding apparatus according to Claim 27, further comprising:

second decoding in-progress result storage means for simultaneously reading and writing second decoding in-progress results corresponding to P edges, which are obtained by said second computation means by performing some of the others of said P check node computations, and said P variable node computations.

31. The decoding apparatus according to Claim 30, wherein said second decoding in-progress result storage means stores said second decoding in-progress results corresponding to edges, which are read when some of the others of said P check node computations, and said P variable node computations are performed, in such a manner that 1s of the check matrix are packed closer in the column direction.

32. The decoding apparatus according to Claim 30, wherein said second decoding in-progress result storage means are two single-port RAMs (Random Access Memories).

33. The decoding apparatus according to Claim 32, wherein said single-port RAMs alternately store said second decoding in-progress results in units of said second decoding in-progress results corresponding to P edges of said check matrix.

34. The decoding apparatus according to Claim 32, wherein said two single-port RAMs (Random Access Memories) each read said second decoding in-progress results stored at the same address.

35. The decoding apparatus according to Claim 30, wherein said second decoding in-progress result storage means stores, at the same address, said second decoding in-progress results corresponding to P edges belonging to a unit matrix whose weight is 1, a quasi-unit matrix, or a shift matrix when the sub-matrices whose weight is 2 or more from among the sub-matrices representing said check matrix are represented in the form of the sum of the unit matrix whose weight is 1, the quasi-unit matrix, or the shift matrix.

36. The decoding apparatus according to Claim 27, further comprising:

received information storage means for storing received information of LDPC codes and for simultaneously reading said P pieces of received information.

37. The decoding apparatus according to Claim 36, wherein said received information storage means stores said received information in such a manner that said received information can be read in the sequence necessary for some of the others of said P check node computations, and said P variable node computations.

38. The decoding apparatus according to Claim 27, further comprising:

rearranging means for rearranging first decoding in-progress results obtained by said first computation means by performing some of said P check node computations, or second

decoding in-progress results obtained by said second computation means by performing some of the others of said P check node computations, and said P variable node computations.

39. The decoding apparatus according to Claim 38, wherein said rearranging means comprises a barrel shifter.

40. A decoding method for use with a decoding apparatus for decoding LDPC (Low Density Parity Check) codes, when using as a sub-matrix, a (P × P) unit matrix, a quasi-unit matrix in which one or more 1s, which are elements of the unit matrix, are substituted with 0, a shift matrix in which said unit matrix or said quasi-unit matrix is cyclically shifted, a sum matrix, which is the sum of two or more of said unit matrix, said quasi-unit matrix, and said shift matrix, or a (P × P) 0-matrix, a check matrix of LDPC codes is represented by a combination of a plurality of said sub-matrices, said decoding method comprising:

a first computation step of simultaneously performing P check node computations for decoding said LDPC codes; and

a second computation step of simultaneously performing P variable node computations for decoding said LDPC codes.

41. A program for enabling a computer to decode LDPC (Low Density Parity Check) codes, said program comprising:

a first computation step of simultaneously performing P check node computations for decoding said LDPC codes; and

a second computation step of simultaneously performing P variable node computations for decoding said LDPC codes.